REMARKS

Claims 1-10, 12-14, 16-17, and 20-32 remain in this application. No claims have been added, cancelled, or amended. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §102(e) Rejection - Ellis

The Examiner has rejected claims 1-10 and 12-14 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,191,713 issued to Ellis et al. (hereinafter referred to as "Ellis"). The Applicants respectfully submit that these claims are not anticipated by Ellis.

Claim 1 recites an apparatus comprising "*a first component; a bus coupled with the first component, the bus to transmit packets of data, wherein the packets of data having special cycles embodying control information; and a second component coupled with the bus, the second component to receive the packets of data from the first component via the bus*". Ellis does not teach or suggest these limitations.

As understood by Applicants, Ellis discusses conversion between serial bus cycles and parallel port commands using a state machine. As discussed in the abstract, "*[t]he present invention is directed to a method and apparatus for converting between serial bus cycles and parallel port commands. A serial bus processor processes a serial bus transaction which is represented by the serial bus cycles and is responsive to the parallel port commands. A state machine circuit is coupled to the serial bus processor to provide a plurality of states corresponding to the serial bus transaction. The state machine circuit transitions from one of the states to any one of the states in response to a change condition asserted by a state signal*".

As understood by Applicants, Ellis does not teach or suggest a bus to transmit packets of data having special cycles embodying control information.

Anticipation under 35 U.S.C. Section 102 requires every element of the claimed invention be identically shown in a single prior art reference. The Federal Circuit has indicated that the standard for measuring lack of novelty by anticipation is strict identity.

"*For a prior art reference to anticipate in terms of 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference.*" In Re Bond, 910 F.2d 831, 15 USPQ.2d 1566 (Fed. Cir. 1990).

For at least these reasons, **claim 1** is believed to be allowable over Ellis. **Claims 2-8** depend from claim 1 and are believed to be allowable therefor, as well as for the recitations independently set forth therein.

Independent **claim 9** is believed to be allowable for a similar reason. Dependent **claims 10 and 12-14** depend from claim 9 and are believed to be allowable therefor, as well as for the recitations independently set forth therein.

35 U.S.C. §102(e) Rejection - Hsieh

The Examiner has rejected claims 16-17 and 20-24 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,969,750 issued to Hsieh et al. (hereinafter referred to as "Hsieh"). The Applicants respectfully submit that these claims are not anticipated by Hsieh.

Claim 16 recites a method comprising "*receiving a first signal in a first hub of a hub interface; passing a message in response to the first signal from the first hub via the hub interface, the message having control information; and receiving the message through from the first hub interface in at a second hub*". Hsieh does not teach or suggest these limitations.

As understood by Applicants, Hsieh discusses a moving picture camera with a universal serial bus interface. As discussed in the abstract, "[a*] camera is provided that can be connected to a processing system via an external connector outside of the housing of the processing system. The camera includes a camera housing. An imaging device is provided inside the camera housing that converts moving pictures to a video signal. A bit*

rate reduction circuit is also provided inside the camera housing and connected to the imaging device. The bit-rate reduction circuit reduces a bit rate of the moving picture signal so as to produce a bit-rate reduced video signal having a lower bandwidth than the video signal prior to bit rate reduction".

As understood by Applicants, Hsieh does not teach or suggest "*receiving a first signal in a first hub of a hub interface; passing a message in response to the first signal from the first hub via the hub interface, the message having control information; and receiving the message through from the first hub interface in at a second hub*".

Anticipation under 35 U.S.C. Section 102 requires every element of the claimed invention be identically shown in a single prior art reference. The Federal Circuit has indicated that the standard for measuring lack of novelty by anticipation is strict identity. "*For a prior art reference to anticipate in terms of 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference.*" In Re Bond, 910 F.2d 831, 15 USPQ.2d 1566 (Fed. Cir. 1990).

For at least these reasons, **claim 16** is believed to be allowable over Hsieh. **Claims 17 and 20-21** depend from claim 16 and are believed to be allowable therefor, as well as for the recitations independently set forth therein.

Independent **claim 22** is believed to be allowable for a similar reason. Dependent **claims 23-24** depend from claim 22 and are believed to be allowable therefor, as well as for the recitations independently set forth therein.

35 U.S.C. §102(e) Rejection - Fuoco

The Examiner has rejected claims 25-32 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,594,713 issued to Fuoco et al. (hereinafter referred to as

"Fuoco"). The Applicants respectfully submit that these claims are not anticipated by Fuoco.

Claim 25 recites a chipset comprising "*a memory control hub coupled with a processor and with a memory; a bus coupled with the memory control hub, the bus to transmit packets of data; and an input-output hub coupled with the bus and with an input-output device, the chipset to pass messages between the memory control hub and the input-output hub by transmitting the packets of data on the bus via a hub interface, the messages including control information regarding signals received from and to control at least one of the following: the processor, the memory, and the input-output device*". Fuoco does not teach or suggest these limitations.

As understood by Applicants, Fuoco discusses a hub interface unit and application unit interfaces for expanded direct memory access processor. As discussed in the abstract, "[a]*n expanded direct memory access processor has ports which may be divided into two sections. The first is an application specific design referred to as the application unit, or application unit. Between the application unit and the expanded direct memory access processor hub is a second module, known as the hub interface unit hub interface unit which serves several functions. It provides buffering for read and write data, it prioritizes read and write commands from the source and destination pipelines such that the port sees a single interface with both access types consolidated and finally, it acts to decouple the port interface clock domain from the core processor clock domain through synchronization*".

As understood by Applicants, Fuoco does not teach or suggest "*a memory control hub coupled with a processor and with a memory; a bus coupled with the memory control hub, the bus to transmit packets of data; and an input-output hub coupled with the bus and with an input-output device, the chipset to pass messages between the memory*

control hub and the input-output hub by transmitting the packets of data on the bus via a hub interface, the messages including control information regarding signals received from and to control at least one of the following: the processor, the memory, and the input-output device".

Anticipation under 35 U.S.C. Section 102 requires every element of the claimed invention be identically shown in a single prior art reference. The Federal Circuit has indicated that the standard for measuring lack of novelty by anticipation is strict identity. "*For a prior art reference to anticipate in terms of 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference.*" In Re Bond, 910 F.2d 831, 15 USPQ.2d 1566 (Fed. Cir. 1990).

For at least these reasons, **claim 25** is believed to be allowable over Fuoco. **Claims 30-32** depend from claim 25 and are believed to be allowable therefor, as well as for the recitations independently set forth therein.

Independent **claim 26** is believed to be allowable for a similar reason. Dependent **claims 27-29** depend from claim 26 and are believed to be allowable therefor, as well as for the recitations independently set forth therein.

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: FEB. 3, 2004

Brent E. Vecchia
Reg. No. 48,011

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1030
(303) 740-1980